Remarks

This is a reply to the outstanding Office Action (first action on the merits), dated April 1, 2002, in which concurrently filed herewith is a Petition for Extension of Time covering the two-months extended time period for filing this response including the required fee amount thereto. (An authorized Credit Card Payment Form, covering the fee amount for the extended time period as well as for the additional claim fee, is enclosed herewith.)

In keeping with the outstanding requirement, the title has been amended to be more aptly descriptive of the invention claimed. Acceptance of the same is respectfully requested.

The Specification was revised for purposes of correcting informalities discovered therein as well as to improve the readability thereof. In terms of practicality, applicants are submitting herewith a Substitute Specification (see Attachment A) which is reflective of the changes made therein. Also enclosed herewith is a marked-up version of the original Specification (see Attachment B) showing all the changes being made to the originally submitted Specification. It is submitted, new matter has not been added in connection with the filing of the Substitute Specification, either by addition and/or deletion. Acceptance and formal entry therefor of the accompanying Substitute Specification into the official record is respectfully requested.

By the amendments presented hereinabove, original claims 1, 2, 5 and 6 were amended, non-elected claims 9-16 were canceled but, however, without applicants waiving their right to subsequently file a divisional application directed thereto, and claims 17-32 were newly presented. The amendments made to claims 1, 2, 5 and 6 are strictly directed formal matters including to effect further

clarification of the subject matter being covered as well as improve the readability thereof. The additional claims, namely, claims 17-32, are being presented in consideration of covering various other combinations including particularities thereof that are covered by the previously pending claims including in a manner which is also associated with CMOS (Complementary MOS) transistor arrangements such as depicted with regard to Figs. 4-5 and 6-7 of the drawings, although not limited thereto.

With regard to newly added claim 17, it further limits the "silicon layer" of the stacked gate electrode structure to a polycrystalline silicon layer (e.g., 103 in Figs. 1-3 and 311, 312 in Figs. 5C and 7C). Newly added claim 18 is similar to claim 17 but is dependent instead on original claim 4 and newly added claim 19 is similar to original claim 3 but is dependent instead on newly added claim 18. Newly added claim 20 (dependent on base claim 1) further limits the gate electrode stacked structure in connection with a MOS transistor in which the source as well as the drain region thereof has a first, relatively shallow diffusion layer and a second deep-diffusion layer, in the semiconductor substrate, such as shown in Figs. 5C and 7C, although not limited thereto. Newly added claims 21-23 are similar to newly added claim 17 but are combined differently therefrom, respectively. Newly added claim 24 is similar to claim 7, but is combined differently therefrom.

Newly added claim groups including claims 25+ and 29+ are inclusive of subject matter covered by original claims 1+ and 5+ but, however, further characterize the stacked gate electrode structure in connection with a complementary MOS transistor arrangement.

According to the outstanding Office Action, claims 1-3, 6 and 7 were

rejected under 35 USC §102(e) as anticipated by Weimer et al (US 6,291,868 B1); claim 5 was also rejected under 35 USC §102(e) in view of Weimer et al (supra); and claims 4 and 8 were rejected under 35 USC §103(a) over the teachings of "Weimer et al in view of the remarks." It will be shown, hereinbelow, the invention according to original claims 1-8 and further according to newly added claims 17-32 not only was not disclosed by Weimer et al but, moreover, could not have been suggested therefrom even in view of the Examiner's additional arguments. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

With regard to claims 1+ and 25+, the invention calls for the gate electrode of a MOS transistor or of a CMOS transistor structure to be provided as a stacked structure including a silicon layer, a metal silicide layer, a reaction barrier layer and a metallic layer, formed in that order beginning with the silicon layer. With regard to the first three examples of the present disclosure, gate electrode stacked layers 103, 108, 105 and 106 are related thereto, respectively, and with regard to the fourth and fifth embodiments, gate electrode stacked layers 311 (312), 320, 308 and 307 are related thereto, respectively, although not limited thereto. The semiconductor device scheme according to claims 5+ and 29+ similarly call for a stacked gate electrode structure as that shown by the example embodiments in the present application. It is submitted, such a scheme as that presently called for and as further detailed by the corresponding dependent claims thereof not only was not disclosed by Weimer et al but, moreover, could not have been suggested therefrom, even in a manner as that alleged in the outstanding rejections.

It is alleged in the rejection that Weimer et al disclosed a gate electrode stacking scheme having four layers in which the metallic layer of the present invention is met by layer 116 in Weimer et al. However, a careful study of Weimer's gate electrode stacked structure shows that this is not correct. In order to be able to satisfy the conditions of the present invention, Weimer et al's stacked gate electrode structure must contain a stacking of four layers such as that presently called for, namely, a silicon layer/a metal silicide layer/a reaction barrier layer/and a metallic layer, in that order, with the metallic layer being the uppermost layer of the just referred to four-layered structure. However, with regard to Weimer et al's MOS transistor 12 structure, in Fig. 1, thereof, for example, the vertically stacked gate electrode structure 112 includes three electrically conductive layers (e.g., 100, 102 and 104). (Column 2, lines 58-60, in Weimer et al.) Layer 116 in Fig. 1 of Weimer et al corresponds to the insulating cap layer which is a vapor deposited SiO_2 or Si_3N_4 insulating material.

According to Weimer et al's stacked gate electrode structure 112, the bottom conductive layer 104 thereof may be a silicon or polysilicon layer, of a number of disclosed examples thereof; the top conductive layer, which is layer 100, includes a low-resistivity material which can be metal or metal silicide; and the intervening layer 102 is a conductive diffusion barrier layer. (Column 2, line 65, to column 3, line 5, in Weimer et al.) It is clearly apparent that Weimer et al failed to disclose a gate electrode with a four-layered stacked structure such as that presently called for in claims 1+, 5+, 25+ and 29+. In fact, Weimer et al also failed to suggest the formation of a four-layered stacked structure as that presently called which requires a silicon layer/metal silicide layer/a reaction barrier layer/a metallic layer including various other details thereof called for by

the corresponding dependent claims thereof.

According to Weimer et al's teachings, such as shown with regard to Fig. 1 of the drawings, there is formed on the gate oxide insulating film 106, a polysilicon (silicon) 104, a barrier layer 102 is formed thereon and a conductive layer 100 is formed on the barrier layer 102 and an insulating layer 116 is formed on the conductive layer 100. Weimer et al did disclose that the intervening layer 102 of the stacking arrangement 112, may be that of a metal silicide, a metal nitride, or a metal silicide nitride in an alternative sense (see column 3, lines 14-23 thereof). And with regard to the uppermost conductive layer 100, according to Weimer et al, it may be formed of either a metal layer or a metal silicide layer (see column 3, lines 52-60, in Weimer et al). It is submitted, Weimer et al neither disclosed nor suggested laminating (stacking) a four-layered gate electrode structure including, from the bottom upwardly, a silicon layer/metal silicide layer/reaction barrier layer/metallic layer, as that presently called for, nor, for that matter, according to the further details as it relates to that four-layered gate electrode structure. For the same and similar reasons as that argued above, therefore, the invention according to the dependent claims also could not have been achieved from Weimer et al's teachings.

Therefore, in view of the amendments presented hereinabove, together with these accompanying remarks, reconsideration and favorable action on all of the presently pending claims (claims 1-8 and 17-32) and an early formal notification of the allowability of the above-identified application are respectfully requested.

Applicants would also like to bring to the USPTO's attention the following two (2) uncovered art documents: US 2002/0008294 A1 to Hayashi et al and US

6,306,743 B1 to Lee, in keeping with the duty of disclosure/candor requirements. Copies of these art documents are enclosed herewith together with a listing therefor of the same in equivalent form PTO 1449 for the Examiner's consideration and in accordance with the requirements under 37 CFR §1.97, regarding the filing of an Information Disclosure Statement (IDS). In addition to the submission of these documents as well as a listing therefor in equivalent form PTO 1449, enclosed herewith is a certified English translation of the priority Japanese patent application corresponding to the above-identified application. The certified English translation, which establishes a supportive basis of the disclosure of the above-identified application in connection with the earlier filed priority Japanese application, listed in the original Declaration of the present application, is being submitted to render the above-named Hayashi et al and Lee documents inapplicable as prior art references with regard to the present claimed subject matter. Specifically, since the priority Japanese application of the present application has a filing date of April 14, 2000, which is earlier than the effective U.S. filing dates and of also the priority dates associated with Hayashi et al and Lee, they may not be admitted as prior art in view of the filing of the accompanying certified English translation of the priority Japanese application of the present application. The certified English language translation, it is submitted, establishes clear support of the present claimed subject matter prior to the effective dates of both Hayashi et al and Lee. The submission of translations of the priority application in a U.S. application for purposes of overcoming the date of a reference is permitted under 37 CFR §1.55(a)(4).

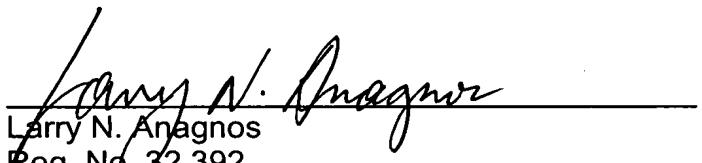
If the USPTO determines that a charge is appropriate with the filing of these two art documents noting that they are also being listed in equivalent form

PTO 1449, the USPTO is authorized to charge the below-named Law Firm's Deposit Account regarding the appropriate fee directed thereto.

A marked-up version showing changes made is enclosed herewith.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (500.40010X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



Larry N. Anagnos
Reg. No. 32,392

LNA/dks
703-312-6600

MARKED-UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS:

Please **amend** claims 1, 2, 5 and 6 to read as follows:

1. (Amended) A semiconductor device with an MOS transistor, [where the] wherein a gate electrode of the MOS transistor is [in] provided as a stacked structure comprising a silicon layer, a metal silicide layer, a reaction barrier layer and a metallic layer, formed in [this] that order [from the bottom upwards] beginning with the silicon layer.

2. (Amended) A semiconductor device according to Claim 1, wherein the silicon layer is doped with an impurity of any desired [conductor] conductivity type.

5. (Amended) A semiconductor device with an MOS transistor whose gate electrode is [in] provided as a stacked structure comprising a silicon layer and a metallic layer as [an] the uppermost layer thereof, [provided above the silicon layer,] wherein a metal silicide layer is provided on the silicon layer side and a reaction barrier layer is provided under the metallic layer side between the silicon layer and the metallic layer.

6. (Amended) A semiconductor device according to Claim 5, wherein the silicon layer is doped with an impurity of any desired [conduction] conductivity type.